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Power Reduction Analysis using Dual Threshold Voltage Domino Logic

R Jeyaramapriya
Department of Electronics and Communication Engineering
Sivanthi Aditanar College of Engineering
Tiruchendur, Tamilnadu, India
Jeyaramapriya.rjp@gmail.com

S P Valan Arasu
Department of Electronics and Communication Engineering
Sivanthi Aditanar College of Engineering
Tiruchendur,Tamilnadu, India

***Abstract*- Dual threshold voltages domino design methodology utilizes low threshold voltages for all transistors that can switch during the evaluate mode and utilizes high threshold voltages for all transistors that can switch during the precharge modes. Employed standby switch can strongly turn off all of the high threshold voltage transistors which enhance the effectiveness of a dual threshold voltage CMOS technology to reduce the sub threshold leakage current. Sub threshold leakage currents are especially important in burst mode type integrated circuits where the majority of the time for system is in an idle mode. The standby switch allowed a domino system enters and leaves a low leakage standby mode within a single clock cycle. In addition, we combined domino dynamic circuits style with pass transistor XNOR and CMOS NAND gates to realize logic 1 output during its precharge phase, but not affects circuits operation in its evaluation and standby phase. The first stage NAND gates output logic 1 can guarantee the second stage computation its correct logic function when system is in a cascaded operation mode. The simulation results demonstrated with the help of MICROWIND software. Carry look-ahead adder is designed at the transistor level with reduced chip area, power consumption and propagation delay time more than 40%, 45% and around 20% respectively.**

Keywords- Complementary metal oxide semiconductor (CMOS), Carry look ahead adder (CLA), Programmable logic Array (PLA), V_{th}- Threshold Voltage

I. INTRODUCTION

With the rapid growth of the portable electronics market in the last few years, the emphasis in VLSI design is shifting from high speed to low power. Portable applications like wireless communication and imaging systems (digital diaries, smart cards) demand high-speed computations, complex functionalities, and often real-time processing capabilities along with low power consumption.

Traditional approaches to minimizing the power consumption of static complementary metal-oxide-semiconductor (CMOS) logic networks have advocated straightforward reduction in the supply voltage. Since the dynamic power is proportional to the square of the supply voltage, this is the most effective technique for power reduction. The resulting increase in delay can be effectively compensated through increased data-path parallelism in special-purpose signal-processing applications and by careful transistor sizing [1], [2]. In some situations it has been recommended that the threshold voltage of the transistors be reduced to improve the circuit performance [3], [4]. However, the static power component of the power dissipation has an inverse exponential dependency on the threshold voltage. This implies that reducing the threshold voltage could cause a significant increase in the static power component. Methodologies for minimizing the sum total of static and dynamic energy consumption in general-purpose CMOS circuits have been proposed in [5- 7]. Total power is minimized through careful selection of supply and threshold voltage values and device sizes such that the leakage and switching components of the dissipation are equal.

The use of dual-threshold voltages for power reduction has been examined in [8] and [9]. In both the methods, all the transistors in the circuit are initially set to have a low threshold voltage. Subsequently, using the algorithms developed, the threshold voltage of some of the gates that do not lie on critical paths is increased. The leakage power can be reduced by up to 50% without affecting the performance of the circuit.

The sleep switch dual-V_{th} circuit technique strongly turns off all of the high-V_{th} transistors; thereby, exploiting the full effectiveness of employing a dual-V_{th} CMOS technology to reduce sub threshold leakage current. The sleep switch circuit technique reduces the sub threshold leakage energy by up to 714 times as compared to a standard dual-V_{th} domino logic circuit. The energy overhead of the circuit technique is low.

II. PROPOSED STANDBY SWITCH DUAL V_{TH} DOMINO LOGIC CIRCUITS

Dual-V_{th} transistors in domino logic circuits for reducing its subthreshold leakage energy consumption, as shown in figure. 1 in which the high threshold voltage (high-V_{th}) transistors are represented by a thick line in its channel region. The technique proposed in [21] utilizes both high and low threshold voltage (low-V_{th}) transistors, high-V_{th} transistors are employed on the noncritical precharge paths, alternatively, low- V_{th} transistors are employed on the speed critical evaluation paths. Dual- V_{th} domino logic circuit techniques with differently standby mode control mechanisms, i.e., circuit techniques to place a domino logic circuits into a low leakage state regardless of the input vector and the initial circuits node voltage states(before the clock is gated) have been proposed in the literature [22–24]. Kursun et al. [22], [23] employed sleep switches to place an idle mode dual- V_{th} domino logic circuit into a low leakage state with low energy and delay overhead, and enters and leaves the standby mode within a single clock cycle.The sleep switch circuit technique reduces the leakage energy by up to 830 times and dual- V_{th} CMOS technology lowers the subthreshold leakage energy by up to 714 times as compared to a standard low- V_{th} domino circuit for an 8-bit domino CLAs.

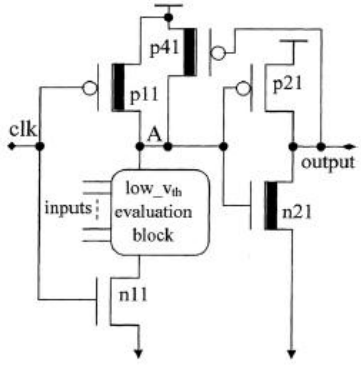

Figure.1. Typical dual-V_{th} domino logic

In order to deal with the difficulty of previous circuits configuration, a low energy and delay overhead dual-V_{th} circuits scheme which employs standby switch to place a dual-V_{th} domino logic circuit into a low leakage state within a single clock cycle was proposed in this paper to lower the sub threshold leakage currents in its idle mode, as shown in figure. 2(b), a high-V_{th} standby switch (an nMOS transistor) n12which is controlled by a separate standby-clock is parallel connected with the low evaluation block that is the discharging path of node A in figure. 2(b), the standby switch can lead the circuits enter and leave its standby mode easily with only a single clock cycle. We also employing CMOS NAND gates instead the output inverter in conventional domino logic to precharge both node A and circuit output to VDD (logic1) during its precharged phase, so the subsequent stage will evaluate its correct logic function in its evaluation phase ,since in circuits precharge operation mode ,the clk =0, p11 and p31 is on, discharging transistor n11 and n31 is off, so that node A and circuit output will be both precharged toVDD by p11andp31,respectively regardless the state of standby-clock. Meanwhile, the CMOSNAND gate output configuration not affect the circuit operation in its evaluation and standby phase, the operation of our proposed dual- V_{th} domino logic circuit is similar to that of the typical dual-V_{th} domino logic circuit apart from the precharge and standby phase.

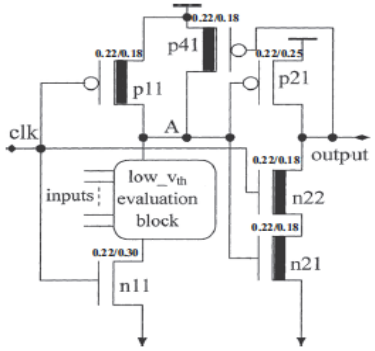

Figure.2. (a) Modified dual V_{th} domino logic circuit

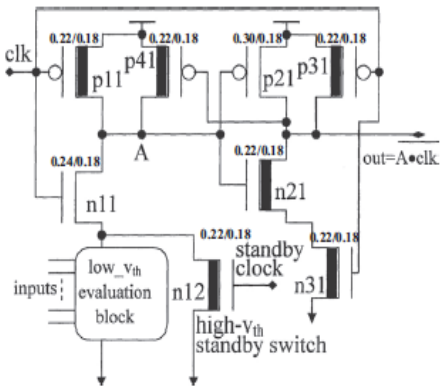

Figure.2. (b) Proposed standby switch dual V_{th} domino logic circuit

During the standby mode of operation, the clock signal is maintained high, turning off the high-V_{th} pull-up transistor 11, p31 and turning on the pull down transistor n11, and n31.The standby-clock transitions high, turning on the standby switch n12. The dynamic node A of the domino gate is discharged through n12 and n11, thereby turning on pMOS transistor p21and turning off the high-V_{th} nMOS transistor rn21 within the output NAND gate, the circuit output transitions high, cutting off the high- V_{th} pMOS "keeper" transistorp41.Following the low-to-high transition of the circuits output, the subsequent gates (fed by the non inverting signals) also evaluate and discharge in a domino fashion. After the node voltages settle to a steady state, all of the high-V_{th} transistors are strongly cut off, significantly reducing the sub threshold leak- age current. Note that this technique requiring no additional gating on the input signals while strongly turning off all of the high-V_{th} transistors within a single clock cycle, is significantly more power, delay, and area efficient as compared to the techniques proposed in [5], [16], [19] and [20]. In addition, as node A with logic0 during the standby mode operation regardless the input vectors of low evaluation blocks, avoided the float state in traditional domino circuits which will cause large leakage current in its output inverters. In traditional domino logic circuits, to ensure that the internal gate node remains at a logic0, the initial inputs into the domino gate must be set high, otherwise, the internal node could float, and cause short circuit currents in the following inverter. Since a float or high dynamic node voltage state is typically the highest leakage state for a dual-V_{th} domino dynamic logic gate since all of the high-V_{th} transistors (other than the pull up transistors) operate in the strong inversion region. As discussed in following section, the advantages of a dual-V_{th} CMOS technology for reducing the leakage current are maximized when all of the high-V_{th} transistors are strongly cut off during its idle mode.

During the evaluation phase, the standby clock is set low, so n12 is cut off, our proposed dual-V_{th} domino dynamic logic circuit operates as a standard dual-V_{th} domino circuits. Since clk=1, p11, p31 is off and n11, n31 is on. If the low-V_{th} evaluation block is evaluated to turn on to the ground ,the node A will be grounded through n11and low-V_{th} evaluation block, i.e., node A discharging to GND (logic0), p21 is on, n21 is off, the circuit output the n is charged to VDD(logic1) by p21. If the low-V_{th} evaluation block is evaluated to cut off to the ground, there will be no discharging path for node A, so node A will maintain its logic1 which is charged during the precharge phase, p21is off, n21 is on, the circuit output discharging to logic 0,a "keeper" pMOS transistor, P41, is added to keep node A at logic1,the circuit output is then latched a logic0. The critical signal transitions of the domino logic circuits are the delay occurring along the evaluation path when node A is discharging, hence, in the dual-V_{th} domino logic circuits, high-V_{th} transistors are used in those non critical precharge paths, alternatively, low-V_{th} transistors must be utilized in the speed critical evaluation paths. As a result, the sub threshold leakage current of the dual-V_{th} domino logic circuits is expected to be smaller compared to an all low-V_{th} domino logic circuits.

Furthermore, our proposed circuit is differ from the traditional domino logic circuits that we connect discharging transistor n11 of low-V_{th} evaluation block from GND in figure. 2(a) to node A in figure. 2(b), this will enhance the body effect of n11,so increase its threshold voltage and decrease its cut off leakage current as discussed in the following section, and move the standby switch n12 from node A in the circuits structure of figure. 1(b) to the source of n11in figure. 1(b) which is the discharging path of low-V_{th} evaluation block, those both can lower the capacitance load effects of node A and enhance the circuits operation speed.

III. CARRY LOOK AHEAD ADDERS DESIGN

Here we present the design of CLA(Carry look-ahead adders) based on our proposed logic family, the structure of basic SUM and CARRY cells used in the design of our long word-length adder circuits are similar to the CMOS adder cells in [25]. Let Ai and Bi be the i^{th} bits of the input data and ci be the carry-in for stage i^{th}, and then we have

$$Gi = Ai \times Bi \quad (1)$$

$$Pi = Ai \times Bi + Ai \times Bi \quad (2)$$

$$Carry = Gi + Pi \times Ci \quad (3)$$

$$Sum = Ci \times Pi + Ci \times Pi \quad (4)$$

where Gi is the carry generate signal and Pi is the carry propagate signal, notably, we define the propagate signals in a different way from the traditional Pi = Ai + Bi, because the $Pi = Ai \times Bi + \overline{Ai} \times \overline{Bi}$ can be re used to generate the SUM term, i.e. Sum's. According to above Boolean equation and utilizing our proposed dual-V_{th} domino logic cells in figure. 2(b), we designed the circuits cells for Gi, Pi, Carry and Sum in our 8-bit CLAs as shown in figure. 3, i.e., figure. 3(a) for Carry's block, figure. 3(b) for Gi's block, and figure. 3(c) for Pi's and Sum's block in which a pass transistor XNOR gate (figure. 3d) is employed to realize $Pi = Ai \times Bi + \overline{Ai} \times \overline{Bi}$, or $Sum = \overline{Ci} \times Pi + Ci \times Pi$ logic functions.

The all transistor size in our designed CLAs were determined individually except specific required transistor with specific size, all high-V_{th} transistor (nMOS/pMOS) with W/L=0.22/0.18, all low-V_{th} nMOS transistor with W/L=0.24/0.18, and all low-V_{th} pMOS transistor with W/L=0.30/0.18

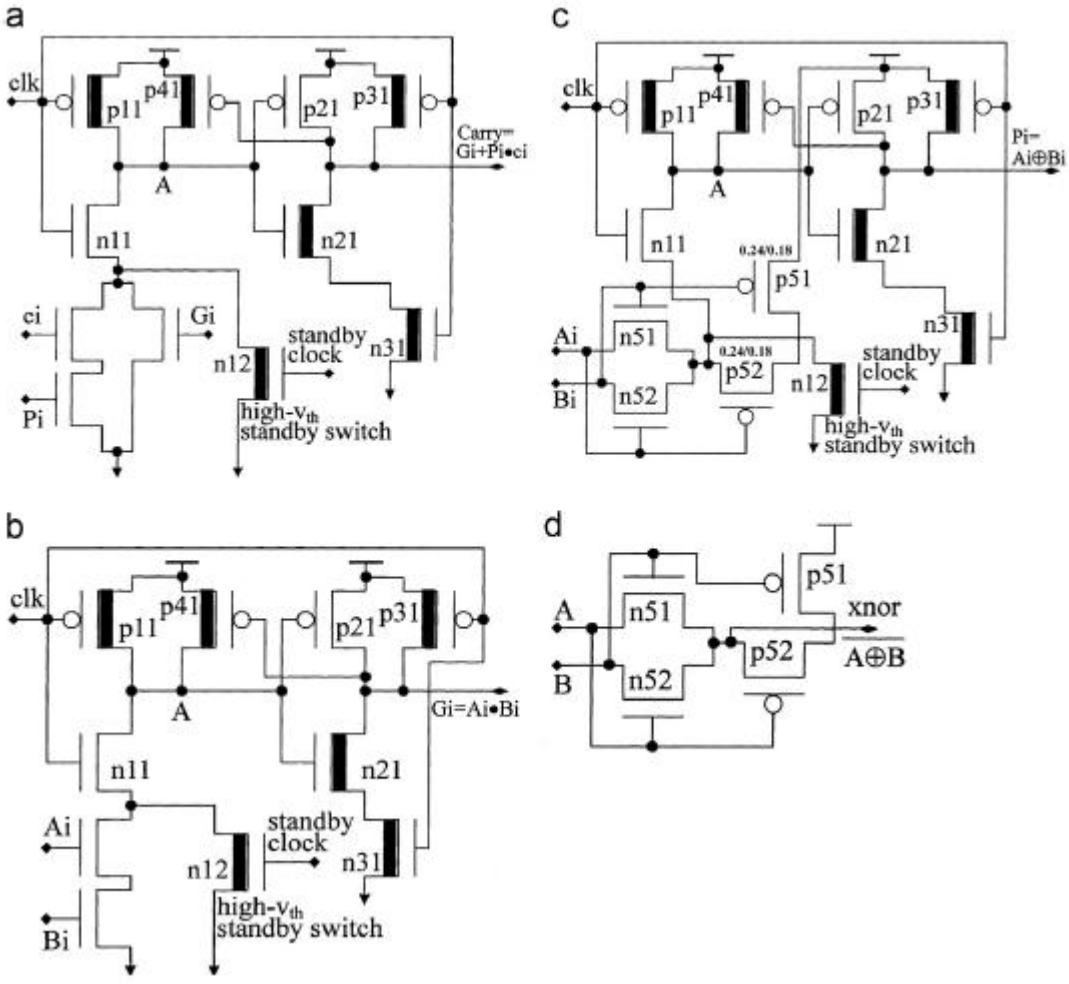

Figure. 3. Carry look-ahead adder circuit cells. (a) Carry's block. (b) Gi's block. (c) Pi's and Sum's block. (d) Pass transistor XNOR gate.

IV. SIMULATION RESULTS

To verify our proposed high performance and low power 8-bit CLAs, MICROWIND simulations were conducted using a 0.18 m technology with simulation condition of VDD=1.8V,. Gi cell in figure. 3(b), Pi and Sum cell in figure. 3(c) and pass transistor XNOR gate in figure. 3(d) were simulated respectively,

The circuits average propagation delay is defined

$$T_{pd} = 1/2\ (t_{pdr} + t_{pdf}) \quad (5)$$

Where, tpdr is the rising propagation delay, from input to rising output crossing, tpdf is the falling propagation delay, from input to falling output crossing. Then, the power values were verified using following formula

$$P_T = C_{pd} \times f_1 \times N_{SW} \times V^2DD \quad (6)$$

Where, P_T is transient power consumption, f_1 is the input signal frequency, N_{SW} is the number of bits switching, and C_{pd} is the dynamic power dissipation capacitance.

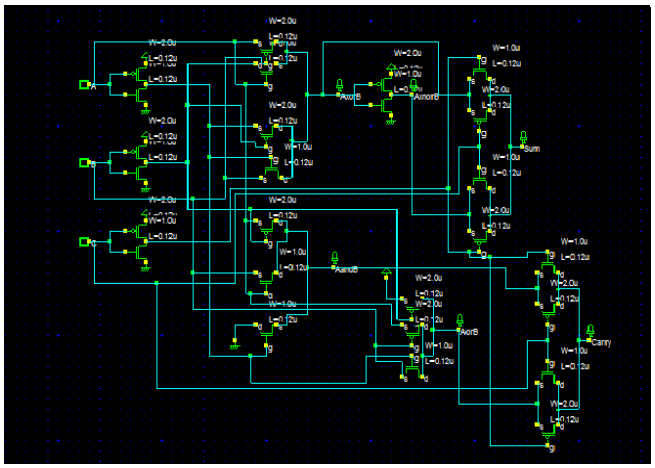

Figure.4. (a) Schematic of CLA in normal mode

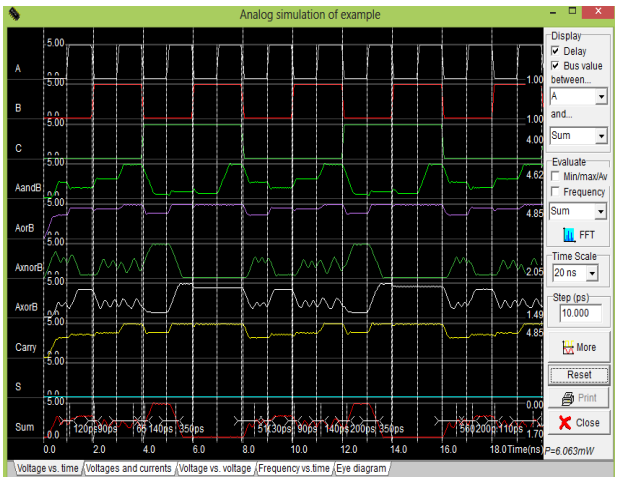

Figure.4. (b) Transient analysis of CLA in normal mode

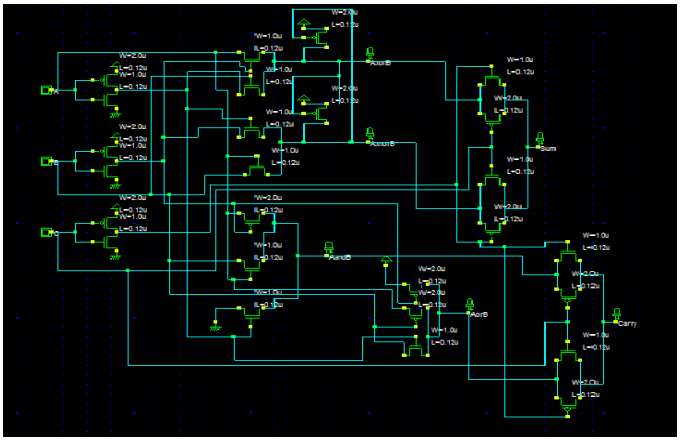

Figure. 4.(c) Schematic of CLA in standby mode

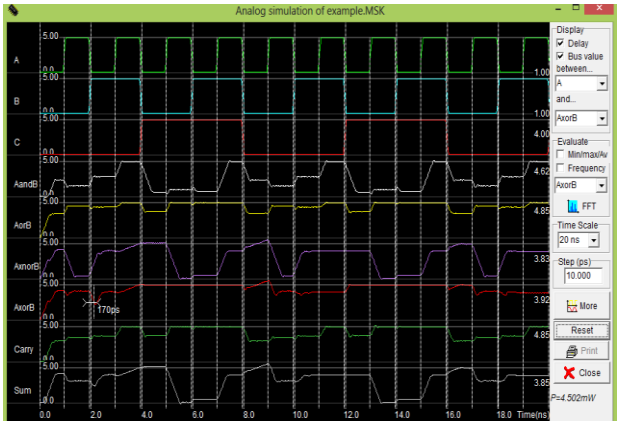

Figure.4. (d) Transient analysis of CLA in standby mode

MODE OF OPERATION	POWER	RISE DELAY	FALL DELAY
NORMAL MODE	6.603 MW	306 PS	216 PS
STANDBY MODE	4.502 MW	170 PS	205 PS

V. CONCLUSION

In this paper, presented an efficient method to minimize power and increase the speed in CLAs design using dual-V_{th} domino logic technique. Sub threshold leakage current can be reduced by using dual threshold voltage domino logic method. The sleep switch transistor can effectively turnoff all the high threshold voltage transistors. MICROWIND simulation has demonstrated that high speed and low power were obtained by our proposed dual-V_{th} domino logic technique, an 8-bitCLAs constructed with our proposed dual-V_{th} domino dynamic logic cells were designed CLAs reduced power consumption more than 15.5% and propagation delay time around 20%.

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